**POORNIMA UNIVERSITY, JAIPUR**

**END SEMESTER EXAMINATION, November 2022**

|  |  |  |  |
| --- | --- | --- | --- |
|  | **4BT7188** | Roll No. \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ | Total Printed Pages: 1 |
| **4BT7188** |  |
| B. Tech. IV Year VII- Semester (Main/Back) End Semester Examination, November 2022  **(EC)** | |
| **BEC07102 : VLSI Design** | | | |

# Time: **3** Hours. Total Marks: **60**

Min. Passing Marks: **21**

Attempt **five** questions selecting one question from each Unit. There is internal choice from Unit I to Unit V. Marks of each question or its parts are indicated against each question / parts. Draw neat sketches wherever necessary to illustrate the answer. Assume missing data suitably (if any) and clearly indicate the same in the answer.

Use of following supporting material is permitted during examination for this subject.

# **1.--------------------------Nil--------------------** **2.------------------Nil-----------------------**

|  |  |  |  |
| --- | --- | --- | --- |
|  |  |  |  |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  | **UNIT-I (CO1)** | **Marks** | **Bloom Level** |
| **Q.1** |  | Explain with neat diagrams the various CMOS fabrication technology. | **(12)** | **Understand** |
|  |  | **OR** |  |  |
| **Q.2** | **(a)** | Explain the operation of PMOS Enhancement transistor. | **(6)** | **Understand** |
|  |  |  |  |  |
|  | **(b)** | What are the advantages of twin tub process? | **(6)** | **Remember** |
|  |  | **UNIT-II (CO2)** |  |  |
| **Q.3** | **(a)** | Define Threshold voltage in CMOS? | **(6)** | **Understand** |
|  |  |  |  |  |
|  | **(b)** | List the basic process for IC fabrication with explanation. | **(6)** | **Remember** |
|  |  | **OR** |  |  |
| **Q.4** |  | Describe in detail twin tub CMOS process of fabrication. | **(12)** | **Understand** |
|  |  | **UNIT-III (CO3)** |  |  |
| **Q.5** | **(a)** | Write short note on CMOS gate transistor sizing. | **(6)** | **Remember** |
|  |  |  |  |  |
|  | **(b)** | Draw the logic diagram of CMOS SR flip flop. | **(6)** | **Create** |
|  |  | **OR** |  |  |
| **Q.6** |  | Draw the CMOS implementation for the following logic gates:  (a) AND (b) OR (c) NAND (d) EX-OR | **(12)** | **Create** |
|  |  | **UNIT-IV (CO4)** |  |  |
| **Q.7** |  | Draw stick diagram layout for 3-input CMOS  (i) NAND gate (ii) Ex-OR gate (iii) NOR gate | **(12)** | **Create** |
|  |  | **OR** |  |  |
| **Q.8** | **(a)** | Describe the layout design style for CMOS circuit design. | **(6)** | **Understand** |
|  |  |  |  |  |
|  | **(b)** | Consider a resistive load inverter circuit with VDD = 5 V, k’n = 20 μA/V2, and VTO = 0.8 V, RL = 200 KΩ, and W/L = 2. Calculate the critical voltages (VOL, VOH, VIL, VIH) on the VTC and find the noise margins of the circuit. | **(6)** | **Evaluate** |
|  |  | **UNIT V (CO5)** |  |  |
| **Q.9** | **(a)** | What is VHDL synthesis? | **(6)** | **Remember** |
|  |  |  |  |  |
|  | **(b)** | Write VHDL code for (i) END Gate (ii0 OR Gate (iii) NAND Gate | **(6)** | **Create** |
|  |  | **OR** |  |  |
| **Q.10** | **(a)** | What is the difference between sequential and combinational circuits? | **(6)** | **Remember** |
|  |  |  |  |  |
|  | **(b)** | Write VHDL code for Full Adder and Half Adder. | **(6)** | **Create** |